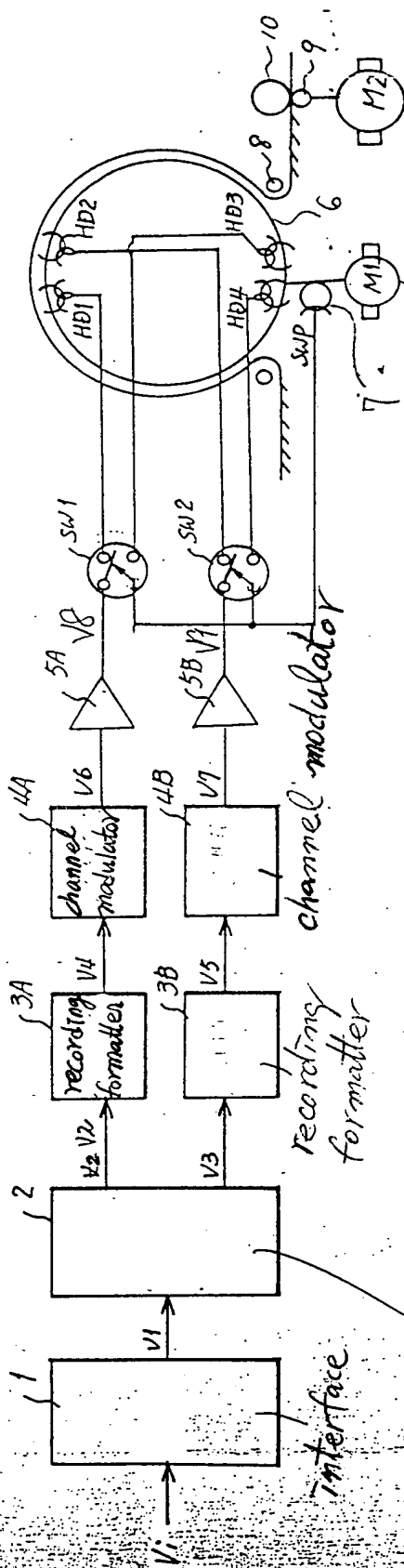


Fig. 1



interleaving and channel-dividing circuit

Fig. 3

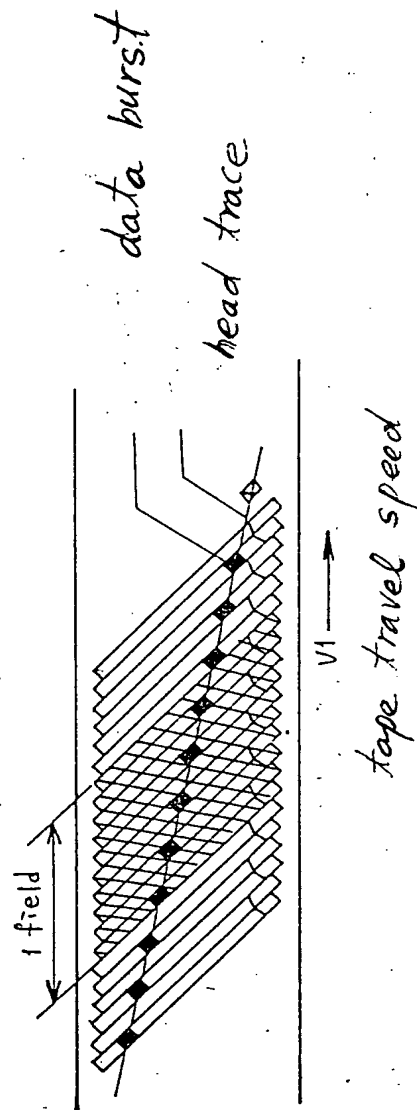


Fig. 2 sync-detecting-
error-correcting circuit

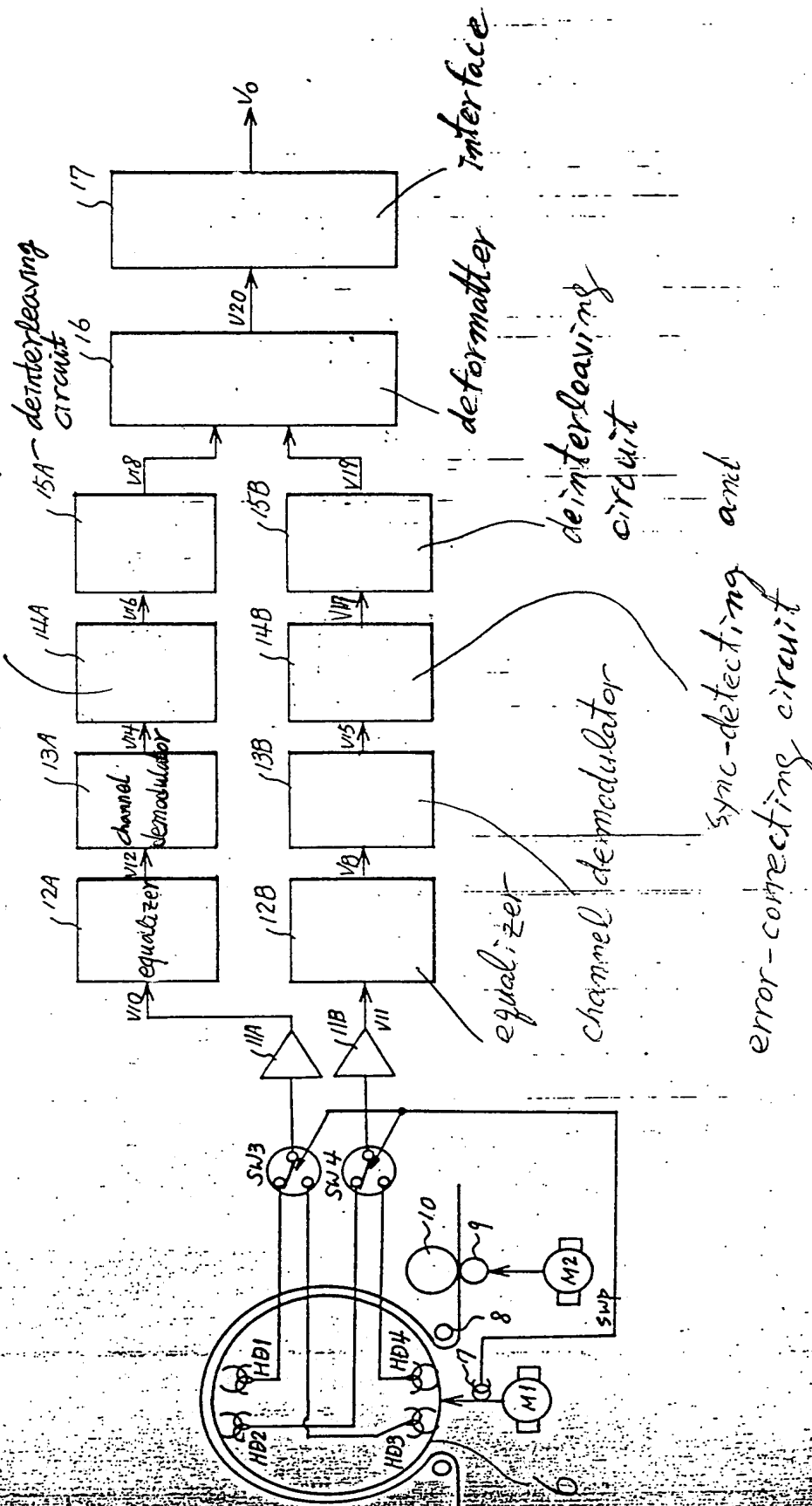


Fig. 4
I-frame

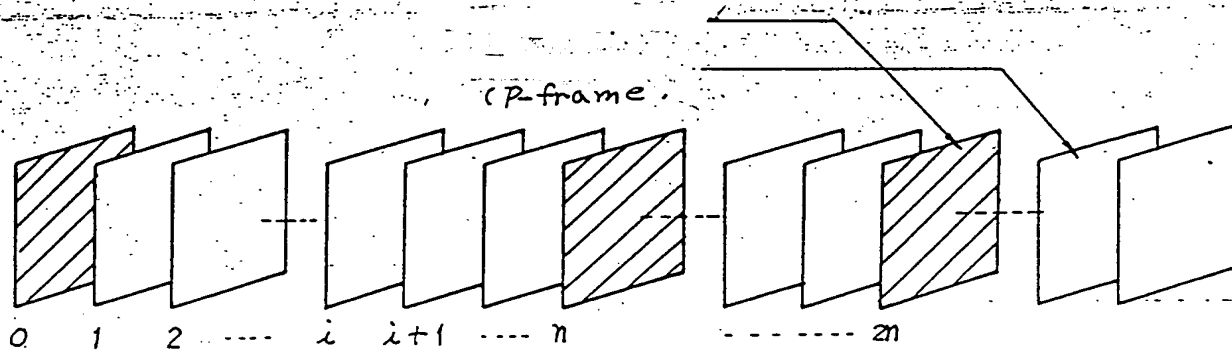


Fig. 5

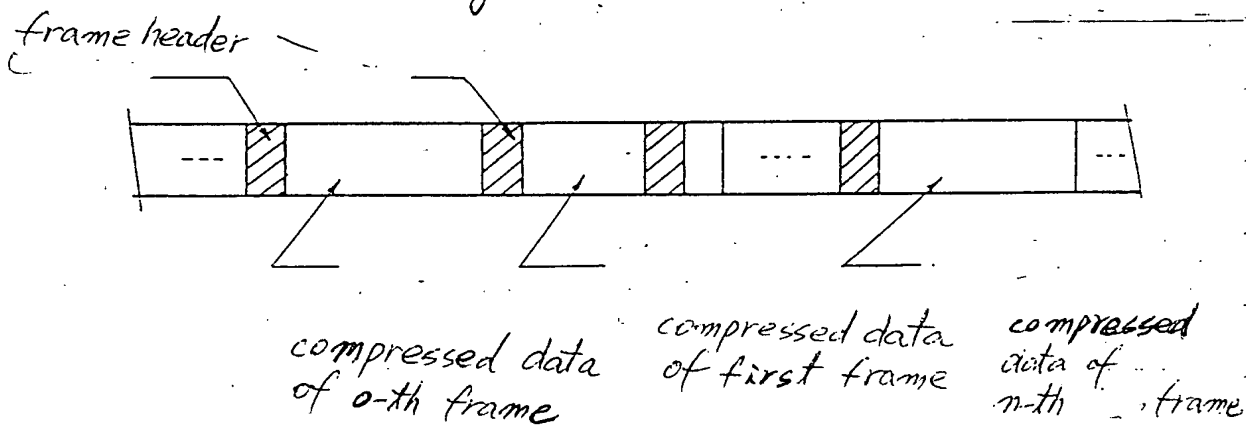
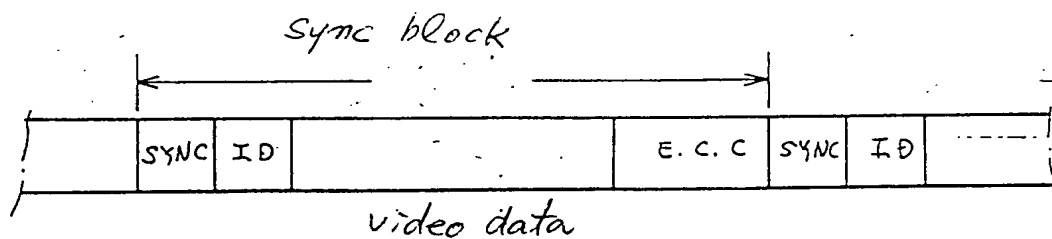
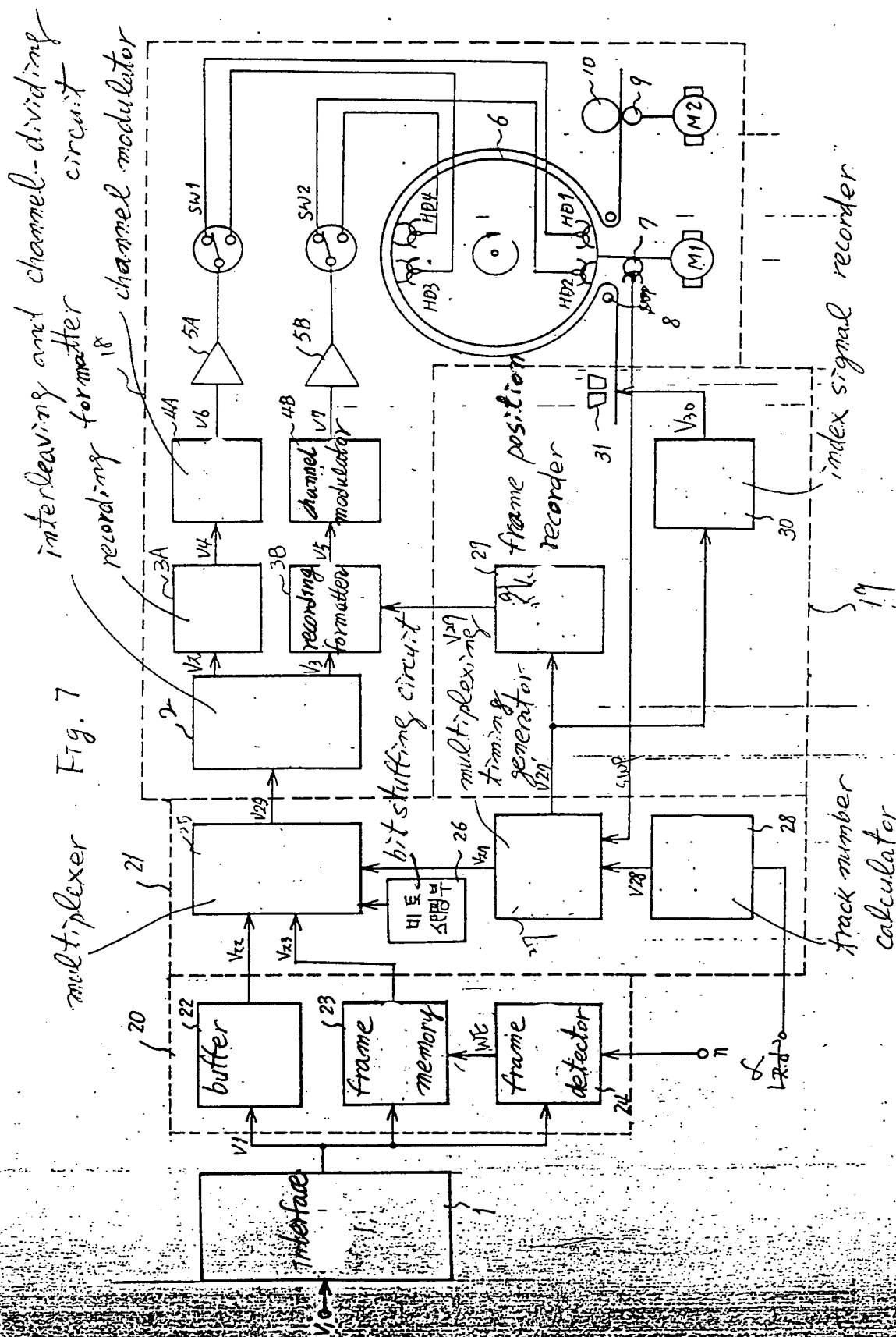
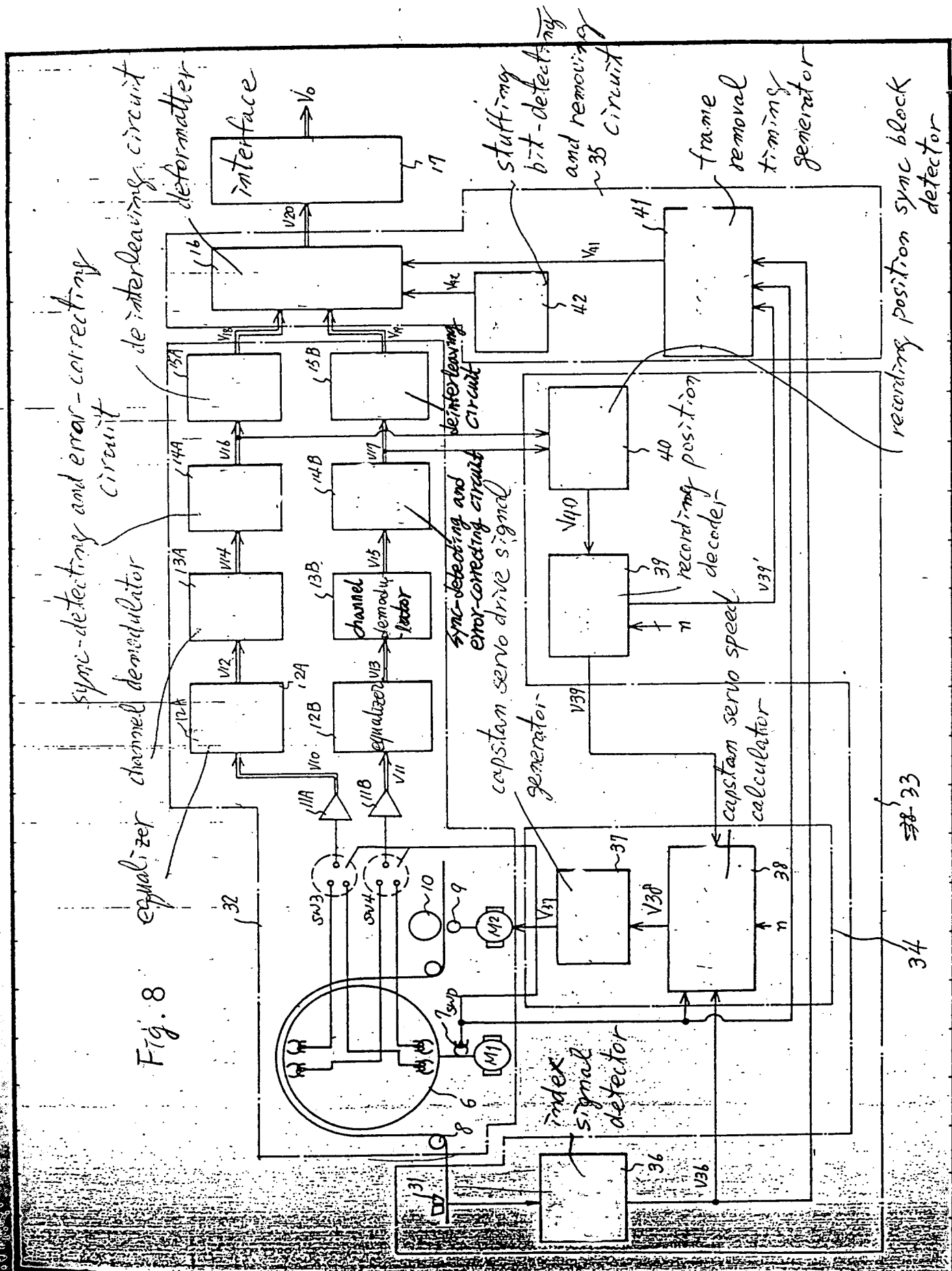
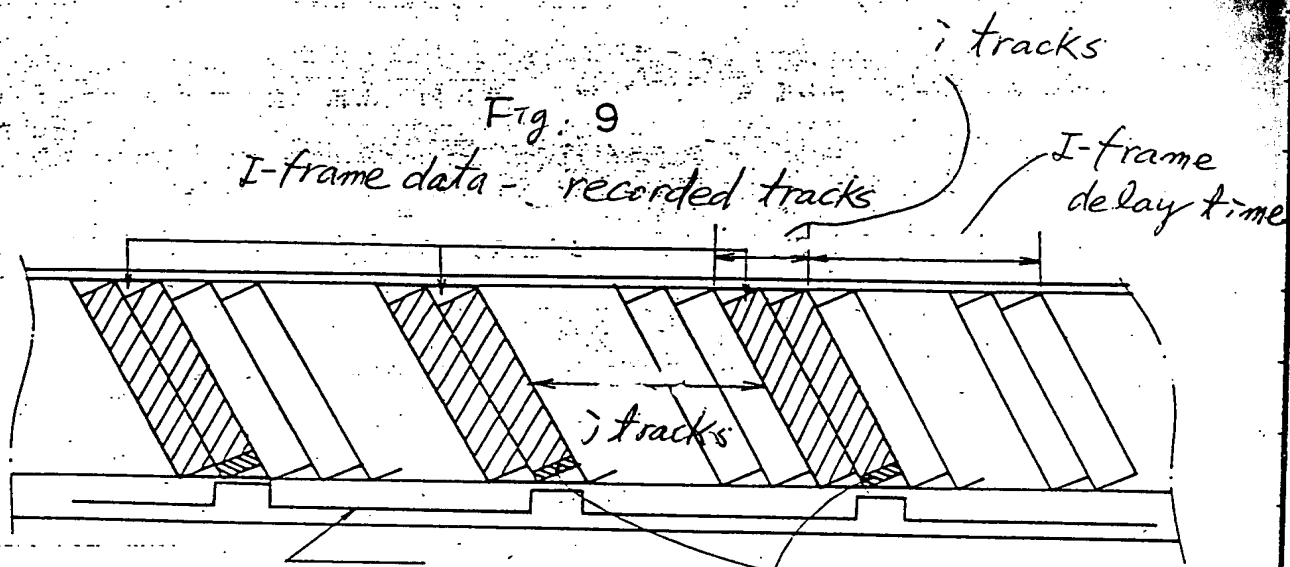


Fig. 6









index information

I-frame position
information sync
block

Fig. 10

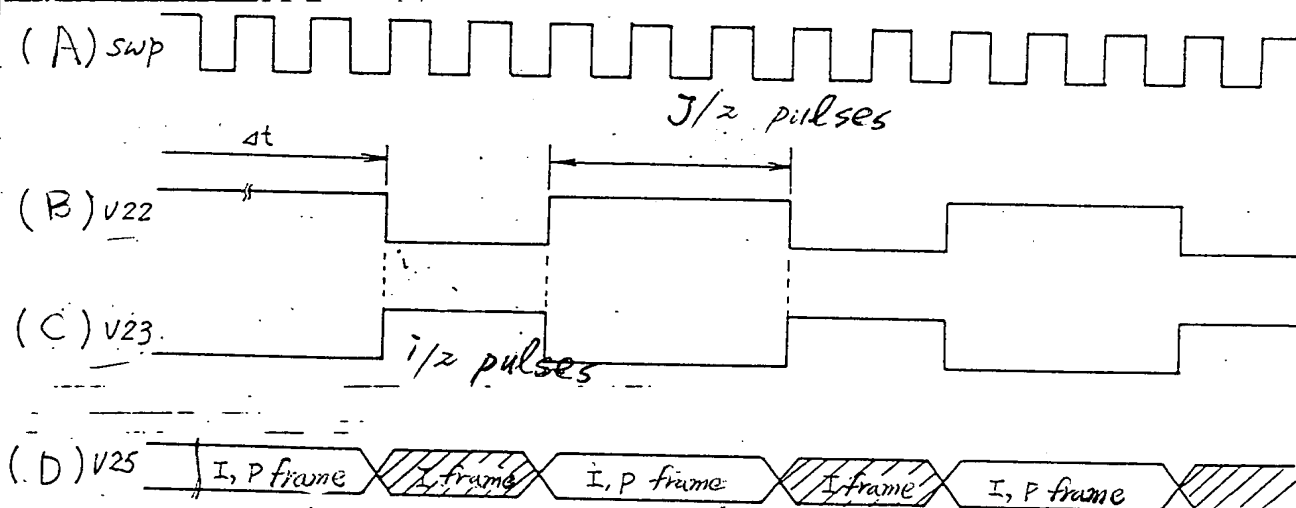
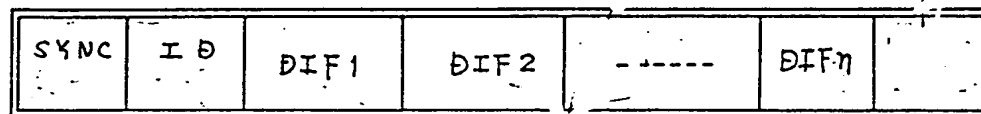


Fig. 11



* Note: DIF 1: Code indicative of number of tracks present between current track and next track including specific data.
 DIF 2: " second track "
 DIF n: " n-th track "

Fig. 12

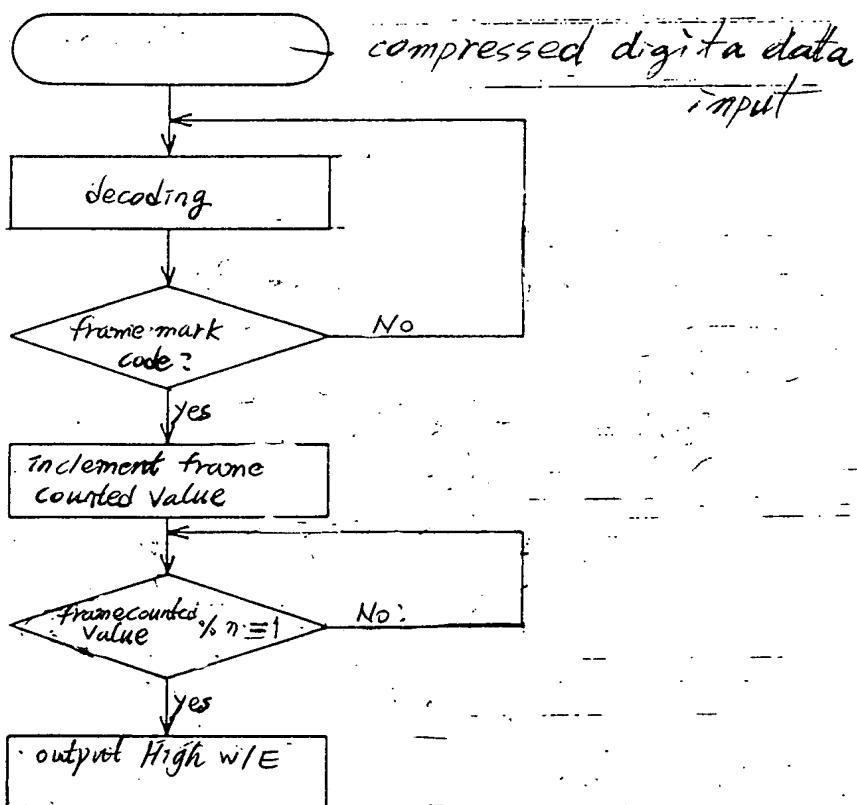


Fig. 13

travel (tracks)

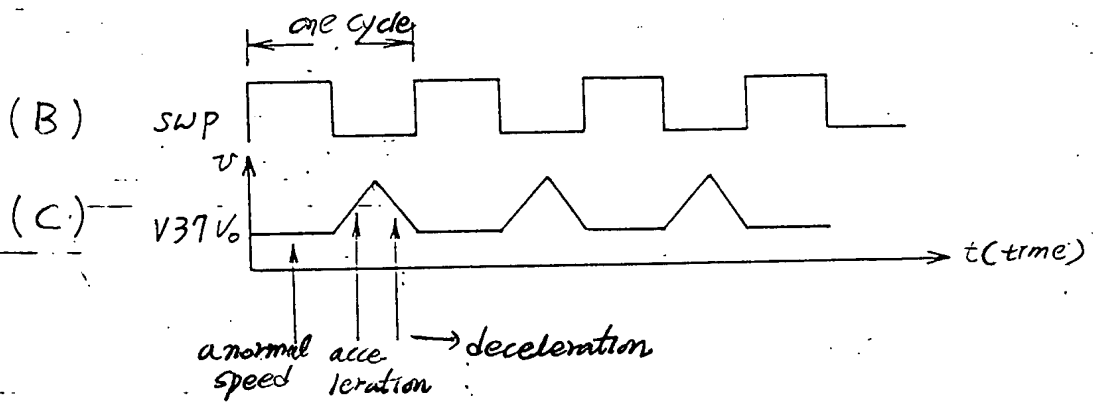
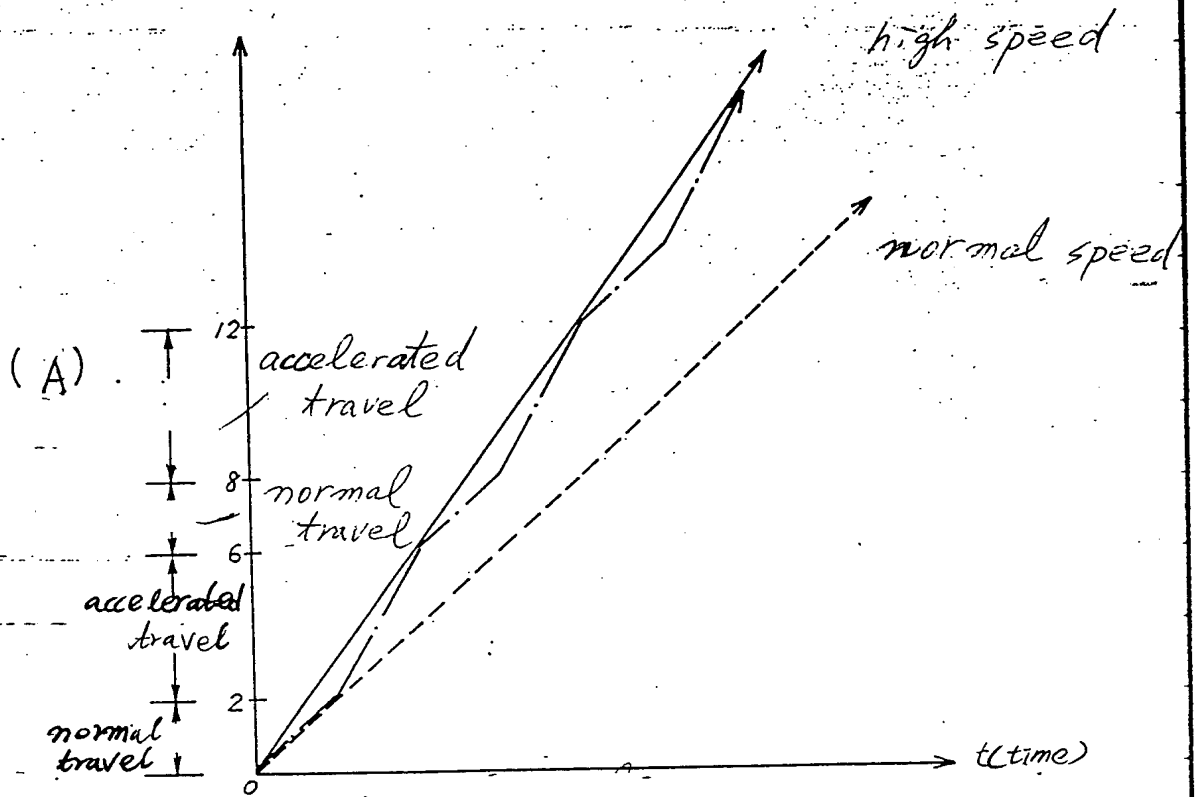


Fig. 14

